Electrical, Electronic and Digital Principles (EEDP)

Lecture 4

Other BJT Biasing Techniques, Design, and CE Amplifier

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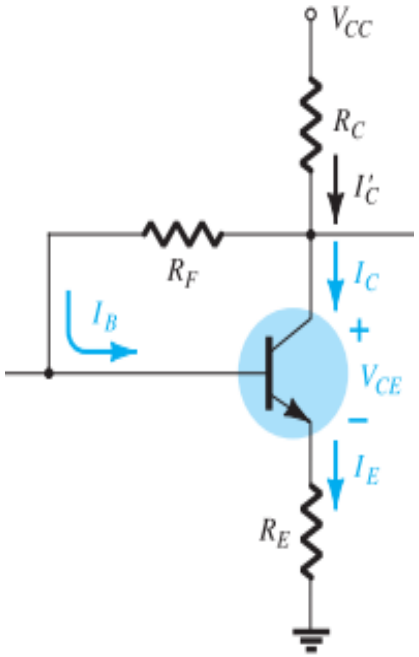
3. Collector-Feedback Bias

- ✓ The collector voltage provides the bias for the B-E junction.
- ✓ The negative feedback creates an "offsetting" effect that tends to keep the Q-point stable.
- ✓ Although the Q -point is not totally independent of beta (even under approximate conditions), the sensitivity to changes in beta or temperature variations is normally less than encountered in other three types



➢ Base–Emitter Loop

$$V_{CC} - I'_C R_C - I_B R_F - V_{BE} - I_E R_E = 0$$

$$I'_C = I_C + I_B$$

However, the level of Ic and Ic' far exceeds the usual level of IB

$$I'_C \cong I_C$$

Substituting $I'_C \cong I_C = \beta I_B$ $\qquad I_E \cong I_C$

The new equation is : $V_{CC} - \beta I_B R_C - I_B R_F - V_{BE} - \beta I_B R_E = 0$

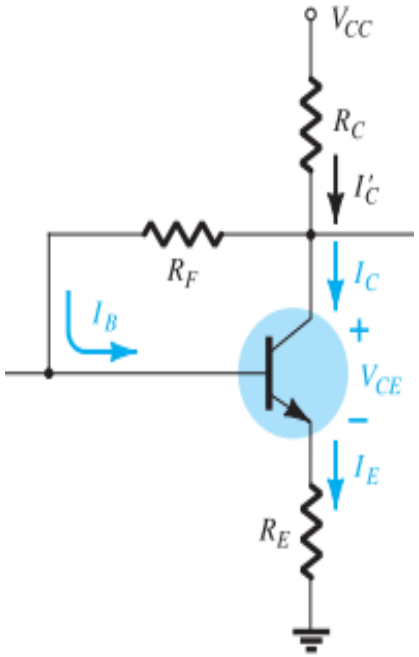
Gathering terms, we have $V_{CC} - V_{BE} - \beta I_B (R_C + R_E) - I_B R_F = 0$

and solving for I_B yields

$$I_B = \frac{V_{CC} - V_{BE}}{R_F + \beta(R_C + R_E)}$$

3. Collector-Feedback Bias

$$I_B = \frac{V_{CC} - V_{BE}}{R_F + \beta(R_C + R_E)}$$



This can be written as:

$$I_B = \frac{V'}{R_F + \beta R'}$$

Because $I_C = \beta I_B$,

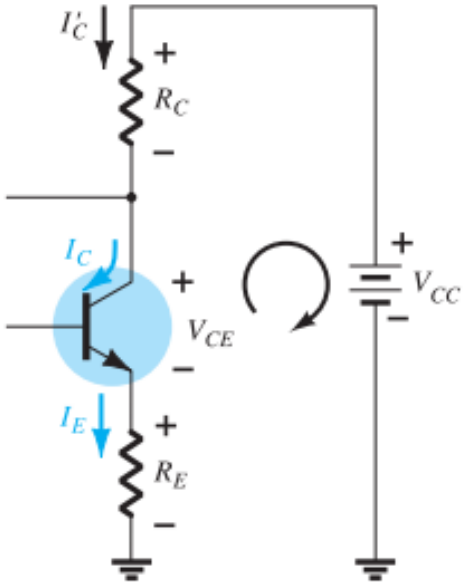
$$I_{C_Q} = \frac{\beta V'}{R_F + \beta R'} = \frac{V'}{\frac{R_F}{\beta} + R'}$$

In general, the larger R' is compared with $\frac{R_F}{\beta}$, the more accurate the approximation that

$$I_{C_Q} \cong \frac{V'}{R'}$$

✓ The result is an equation absent of B_{DC}, which would be very stable for variations in B_{DC}.

3. Collector-Feedback Bias



Output Loop Equation

$$I_E R_E + V_{CE} + I'_C R_C - V_{CC} = 0$$

Because $I'_C \cong I_C$ and $I_E \cong I_C$, we have

$$I_C(R_C + R_E) + V_{CE} - V_{CC} = 0$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

Other Biasing :

EMITTER-FOLLOWER CONFIGURATION

COMMON-BASE CONFIGURATION

4.11 DESIGN OPERATIONS

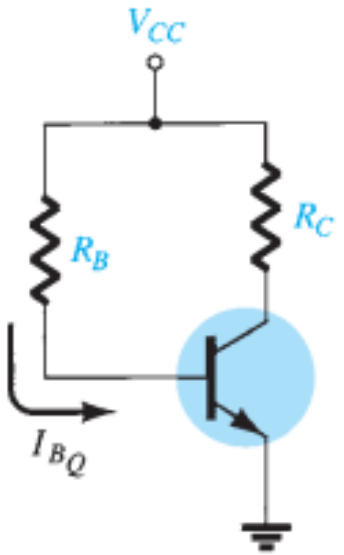
Electronic Devices and Circuit Theory
11th Ed, Boylstd

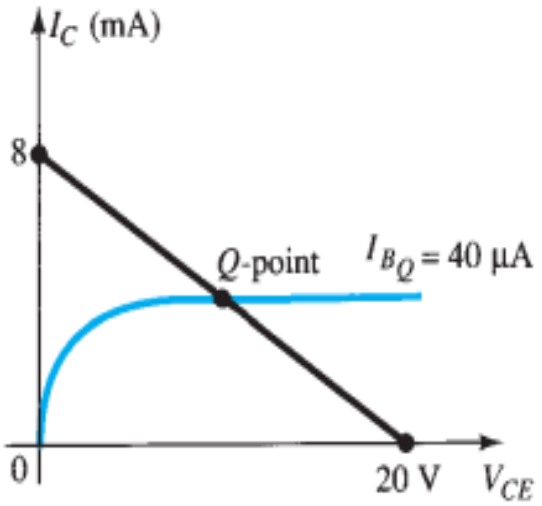
- The design process is one where a current and/or voltage may be specified and the elements required to establish the designated levels must be determined.
- The path toward a solution is less defined and in fact may require a number of basic assumptions that do not have to be made when simply analyzing a network.

- ✓ If the transistor and supplies are specified, the design process will simply determine the required resistors for a particular design.
- ✓ Once the theoretical values of the resistors are determined, the nearest standard commercial values are normally chosen and any variations due to not using the exact resistance values are accepted as part of the design.
- ✓ This is certainly a valid approximation considering the tolerances normally associated with resistive elements and the transistor parameters.

EXAMPLE 4.21 Given the device characteristics of Fig. 4.59a, determine V_{CC}, R_B, and R_C for the fixed-bias configuration of Fig. 4.59b.

Base Bias (Fixed Bias)





Solution: From the load line

$$V_{CC} = \mathbf{20\ V}$$

$$I_C = \left.\frac{V_{CC}}{R_C}\right|_{V_{CE}=0\ V}$$

$$R_C = \frac{V_{CC}}{I_C} = \frac{20\ V}{8\ mA} = \mathbf{2.5\ k\Omega}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$R_B = \frac{V_{CC} - V_{BE}}{I_B}$$

$$= \frac{20\ V - 0.7\ V}{40\ \mu A} = \frac{19.3\ V}{40\ \mu A}$$

$$= \mathbf{482.5\ k\Omega}$$

Standard resistor values are

$$R_C = 2.4\ k\Omega$$

$$R_B = 470\ k\Omega$$

Using standard resistor values gives

$$I_B = 41.1\ \mu A$$

which is well within 5% of the value specified.

EXAMPLE 4.22 Given that $I_{C_Q} = 2\text{ mA}$ and $V_{CE_Q} = 10\text{ V}$, determine R_1 and R_C for the network of Fig. 4.60.

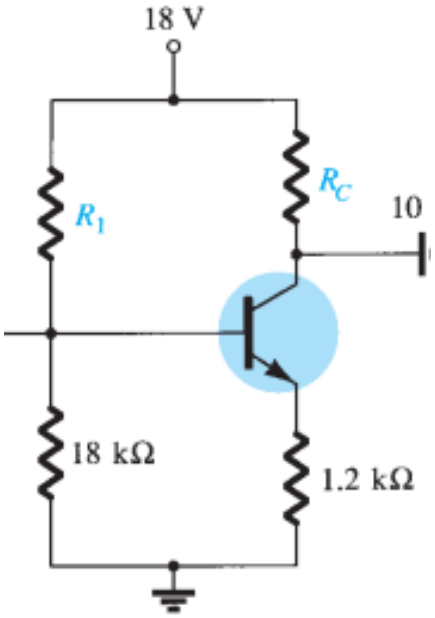
Solution:

$$V_E = I_E R_E \cong I_C R_E$$
$$= (2\text{ mA})(1.2\text{ k}\Omega) = 2.4\text{ V}$$
$$V_B = V_{BE} + V_E = 0.7\text{ V} + 2.4\text{ V} = 3.1\text{ V}$$
$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2} = 3.1\text{ V}$$
$$\frac{(18\text{ k}\Omega)(18\text{ V})}{R_1 + 18\text{ k}\Omega} = 3.1\text{ V}$$
$$324\text{ k}\Omega = 3.1R_1 + 55.8\text{ k}\Omega$$
$$3.1R_1 = 268.2\text{ k}\Omega$$
$$R_1 = \frac{268.2\text{ k}\Omega}{3.1} = \mathbf{86.52\text{ k}\Omega}$$

$$R_C = \frac{V_{R_C}}{I_C} = \frac{V_{CC} - V_C}{I_C}$$

$$V_C = V_{CE} + V_E = 10\text{ V} + 2.4\text{ V} = 12.4\text{ V}$$

$$R_C = \frac{18\text{ V} - 12.4\text{ V}}{2\text{ mA}}$$
$$= \mathbf{2.8\text{ k}\Omega}$$



- The nearest standard commercial values to R1 are 82 k and 91 k .
- However, using the series combination of standard values of 82 k and 4.7 k = 86.7 k would result in a value very close to the design level.

Design Technique to obtain a given specification (operating point)

1. The **supply voltage** and **operating point** were selected from the manufacturer's information on the transistor used in the amplifier.

- ✓ The selection of collector and emitter resistors cannot proceed directly from the information just specified (two unknown quantities (R_C and R_E)]
- ✓ R_E cannot be unreasonably large because the voltage across it limits the range of swing of the voltage Vce
- ✓ The examples examined in this chapter reveal that the voltage from emitter to ground is typically around (1/4) to (1/10) of the supply voltage.

2. Selecting the conservative case (1/10)

emitter-bias

$$V_E = \frac{1}{10}V_{CC} = \frac{1}{10}(20\text{ V}) = 2\text{ V}$$

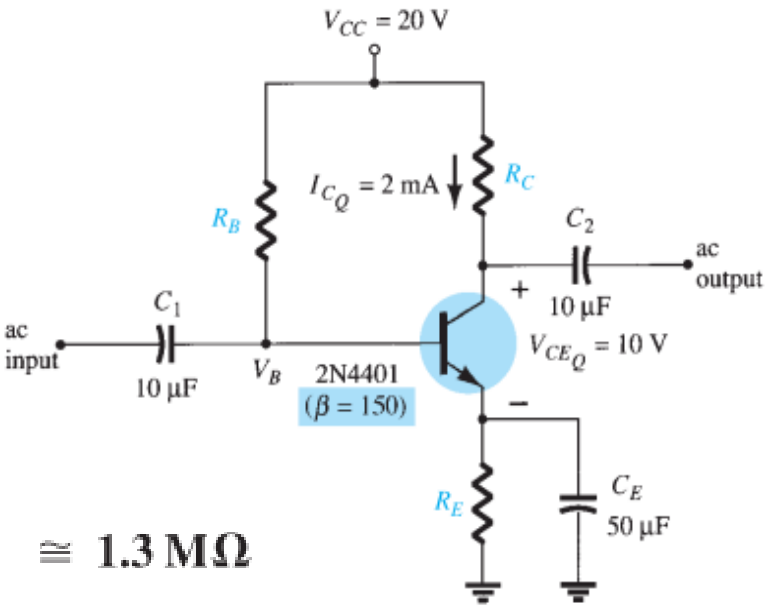
$$R_E = \frac{V_E}{I_E} \cong \frac{V_E}{I_C} = \frac{2\text{ V}}{2\text{ mA}} = \mathbf{1\,k\Omega}$$

$$R_C = \frac{V_{R_C}}{I_C} = \frac{V_{CC} - V_{CE} - V_E}{I_C} = \frac{20\text{ V} - 10\text{ V} - 2\text{ V}}{2\text{ mA}} = \frac{8\text{ V}}{2\text{ mA}}$$

$$= \mathbf{4\,k\Omega}$$

$$I_B = \frac{I_C}{\beta} = \frac{2\text{ mA}}{150} = 13.33\ \mu\text{A}$$

$$R_B = \frac{V_{R_B}}{I_B} = \frac{V_{CC} - V_{BE} - V_E}{I_B} = \frac{20\text{ V} - 0.7\text{ V} - 2\text{ V}}{13.33\ \mu\text{A}} \cong \mathbf{1.3\,M\Omega}$$



Design Technique to obtain a specified operating point

Use the technique for voltage-divider bias

Design of a Current-Gain-Stabilized (Beta-Independent) Circuit

EXAMPLE 4.25 Determine the levels of R_C, R_E, R_1, and R_2 for the network of Fig. 4.63 for the operating point indicated.

$$V_E = \frac{1}{10}V_{CC} = \frac{1}{10}(20\text{ V}) = 2\text{ V}$$

$$R_E = \frac{V_E}{I_E} \cong \frac{V_E}{I_C} = \frac{2\text{ V}}{10\text{ mA}} = \mathbf{200\ \Omega}$$

$$R_C = \frac{V_{R_C}}{I_C} = \frac{V_{CC} - V_{CE} - V_E}{I_C} = \frac{20\text{ V} - 8\text{ V} - 2\text{ V}}{10\text{ mA}} = \frac{10\text{ V}}{10\text{ mA}}$$

$$= \mathbf{1\ k\Omega}$$

$$V_B = V_{BE} + V_E = 0.7\text{ V} + 2\text{ V} = 2.7\text{ V}$$

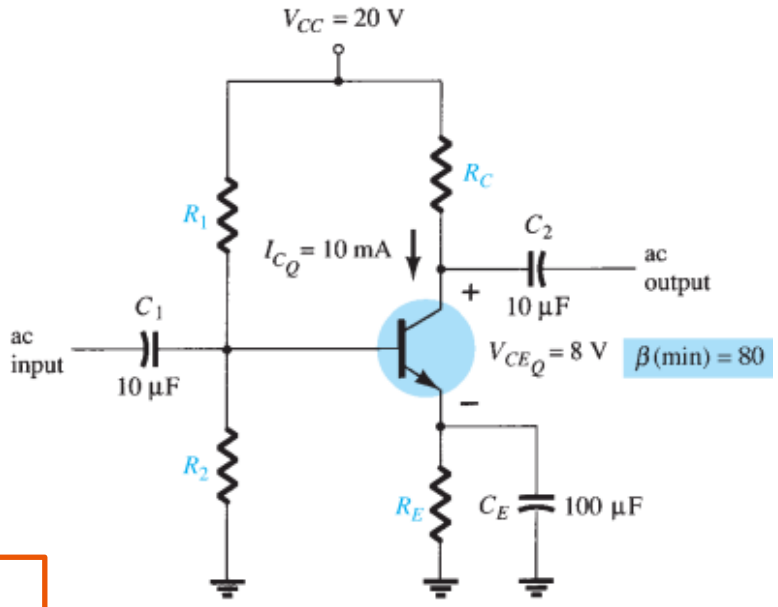


FIG. 4.63
Current-gain-stabilized circuit for design considerations.

✓ Assume that the current through R1 and R2 should be approximately equal to and much larger than the base current (at least 10:1).

$$R_2 \leq \frac{1}{10}\beta R_E$$

$$V_B = \frac{R_2}{R_1 + R_2}V_{CC}$$

$$R_2 \leq \frac{1}{10}(80)(0.2\text{ k}\Omega)$$

$$= \mathbf{1.6\ k\Omega}$$

$$V_B = 2.7\text{ V} = \frac{(1.6\text{ k}\Omega)(20\text{ V})}{R_1 + 1.6\text{ k}\Omega}$$

$$2.7R_1 + 4.32\text{ k}\Omega = 32\text{ k}\Omega$$

$$2.7R_1 = 27.68\text{ k}\Omega$$

$$R_1 = \mathbf{10.25\ k\Omega} \quad (\text{use } 10\text{ k}\Omega)$$

BJT AMPLIFIERS

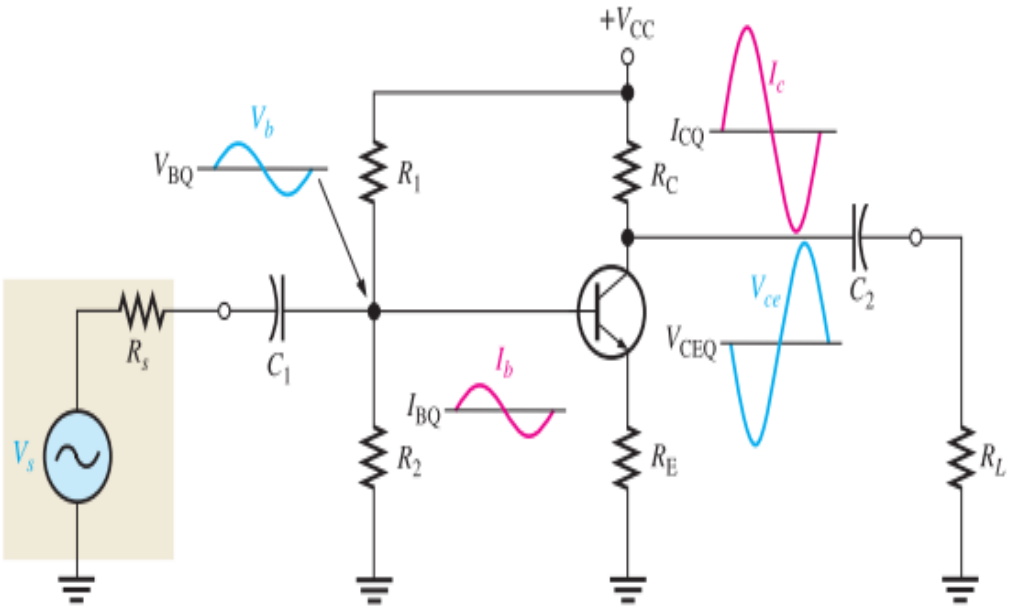
6–1 Amplifier Operation

- The purpose of biasing is to establish a Q-point about which variations in current and voltage can occur in response to an ac input signal.
- In applications where small signal voltages must be amplified such as from an antenna or a microphone—variations about the Q-point are relatively small.
- Amplifiers designed to handle these small ac signals are often referred to as **small-signal amplifiers**.

The Linear Amplifier

A linear amplifier provides amplification of a signal without any distortion so that the output signal is an exact amplified replica of the input signal.

- ✓ The coupling capacitors block dc and thus prevent the internal source resistance, Rs, and the load resistance, RL, from changing the dc bias voltages at the base and collector.
- ✓ The capacitors ideally appear as shorts to the signal voltage.



Amplification in the ac Domain

- ✓ For an amplifying device, the output sinusoidal signal is greater than the input sinusoidal signal, or, stated another way, the output ac power is greater than the input ac power.

$\eta = P_o/P_i$ cannot be greater than 1.

In fact, a *conversion efficiency* is defined by $\eta = P_{o(\text{ac})}/P_{i(\text{dc})}$, where $P_{o(\text{ac})}$ is the ac power to the load and $P_{i(\text{dc})}$ is the dc power supplied.

- ✓ In other words, there is an "exchange" of dc power to the ac domain that permits establishing a higher output ac power.

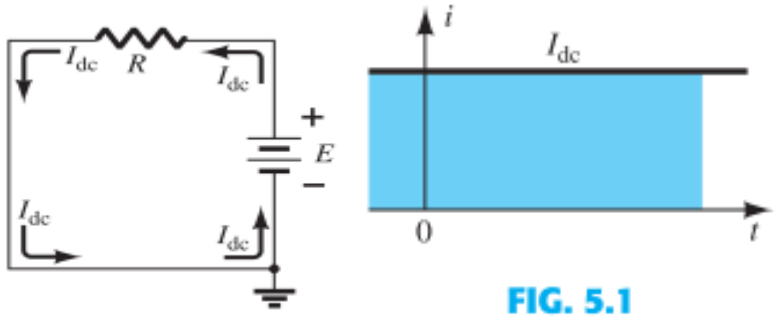


FIG. 5.1
Steady current established by a dc supply.

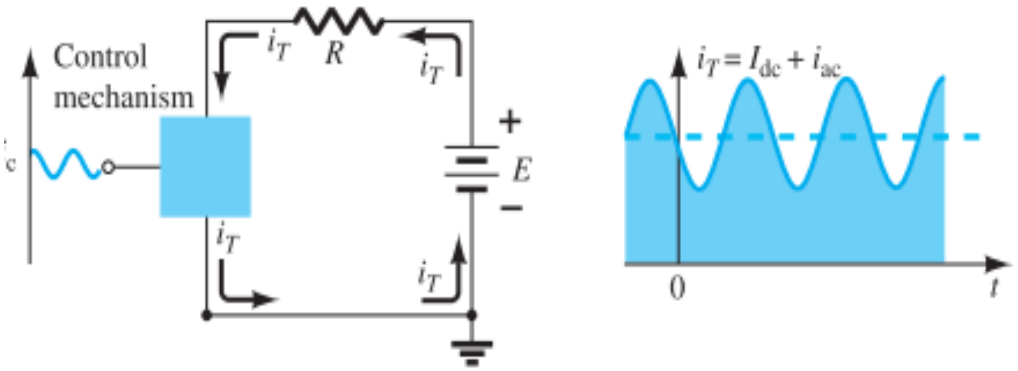


FIG. 5.2
Effect of a control element on the steady-state flow of the electrical system of Fig. 5.1.

Amplification in the ac Domain

$$i_{ac(p\text{-}p)} \gg i_{c(p\text{-}p)}$$

- ✓ The peak value of the oscillation in the output circuit is controlled by the established dc level.
- ✓ Any attempt to exceed the limit set by the dc level will result in a "clipping" (flattening)

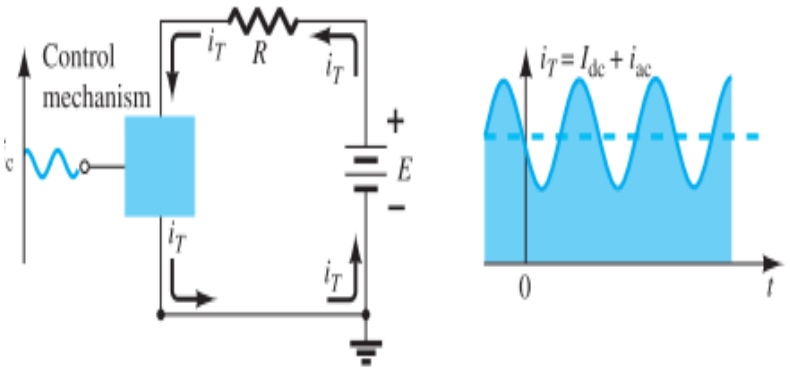


FIG. 5.2

Effect of a control element on the steady-state flow of the electrical system of Fig. 5.1.

The superposition theorem is applicable for the analysis and design of the dc and ac components of a BJT network, permitting the separation of the analysis of the dc and ac responses of the system.

- ➢ Once the dc analysis is complete, the ac response can be determined using a completely ac analysis.
- ➢ However, one of the components appearing in the ac analysis of BJT networks will be determined by the dc conditions(link between the two types of analysis).

6–2 TRANSISTOR AC MODELS

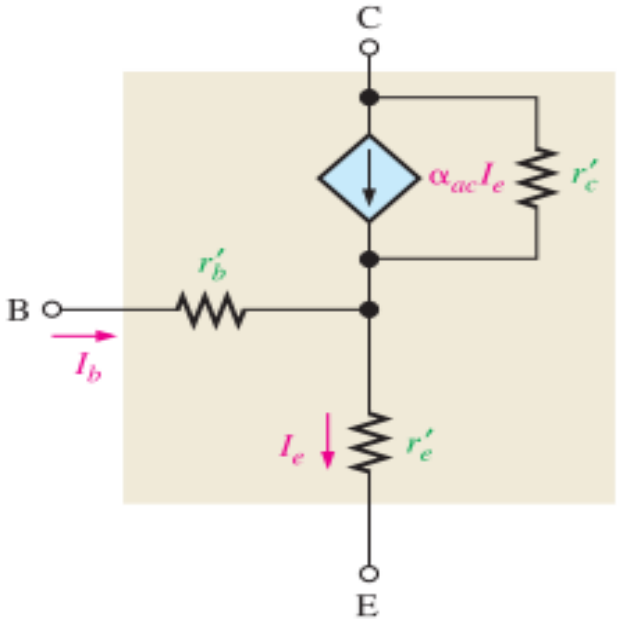
- ✓ To visualize the operation of a transistor in an amplifier circuit, it is often useful to represent the device by a model circuit.

A model is a combination of circuit elements, properly chosen, that best approximates the actual behavior of a semiconductor device under specific operating conditions.

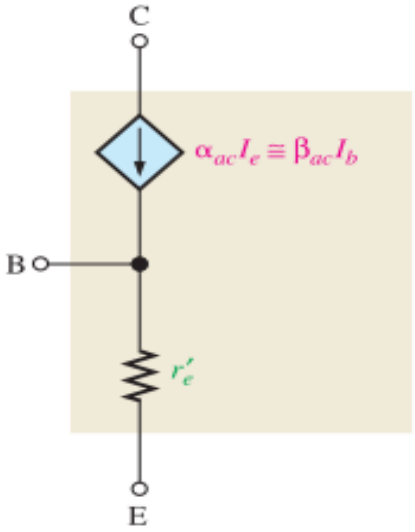
There are three models commonly used in the small-signal ac analysis of transistor

r_e model, the hybrid π model, and the hybrid equivalent model.

r-Parameter Transistor Model



(a) Generalized *r*-parameter model for a BJT

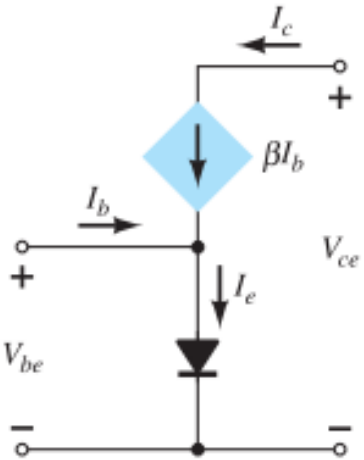


(b) Simplified *r*-parameter model for a BJT

r parameters.

r PARAMETER	DESCRIPTION
α_{ac}	ac alpha (I_c/I_e)
β_{ac}	ac beta (I_c/I_b)
r'_e	ac emitter resistance
r'_b	ac base resistance
r'_c	ac collector resistance

- ✓ The effect of the ac base resistance small enough to neglect
- ✓ (Rc or ro) The ac collector resistance is usually hundreds of kilohms and can be replaced by an open.



Determining r'_e by a Formula

$$r'_e \cong \frac{25\text{ mV}}{I_E}$$

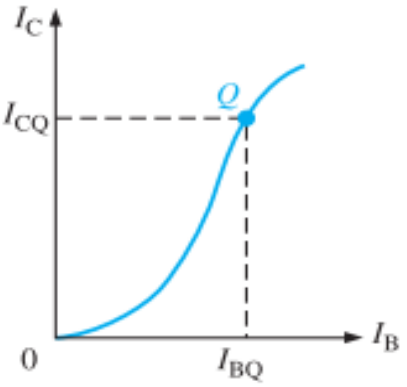
BE Forward diode resistance

Comparison of the AC Beta (β_{ac}) to the DC Beta (β_{DC})

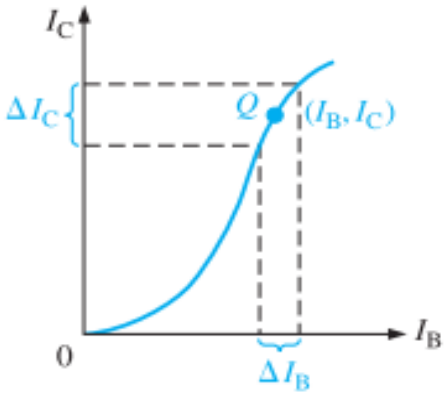
For a typical transistor, a graph of I_C versus I_B is nonlinear, as shown in Figure 6–7(a).

$$\beta_{DC} = I_C/I_B \text{ and } \beta_{ac} = \Delta I_C/\Delta I_B,$$

The values of these two quantities can differ slightly.

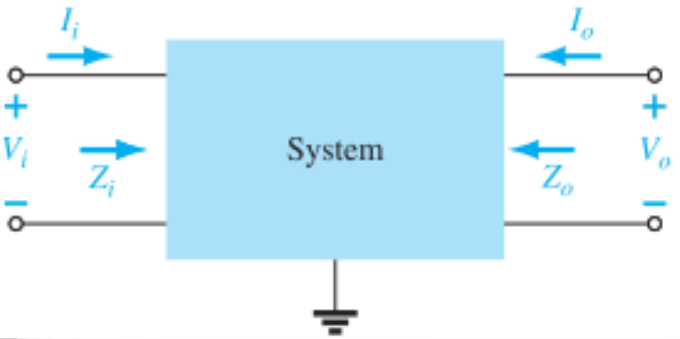


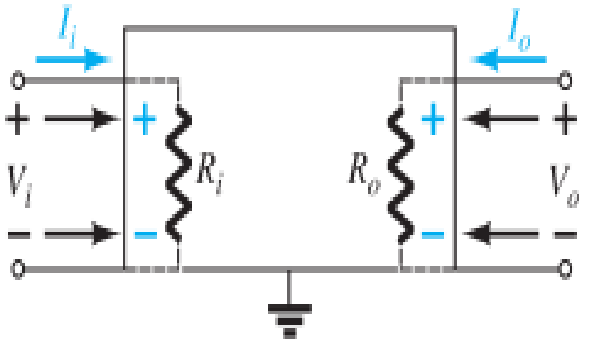
(a) $\beta_{DC} = I_C/I_B$ at Q-point



(b) $\beta_{ac} = \Delta I_C/\Delta I_B$

Input and output resistance of the BJT





Input Resistance at the Base $R_{in(base)}$

- use the simplified r-parameter model of the transistor.
- $Z_i = R_{in(base)}$

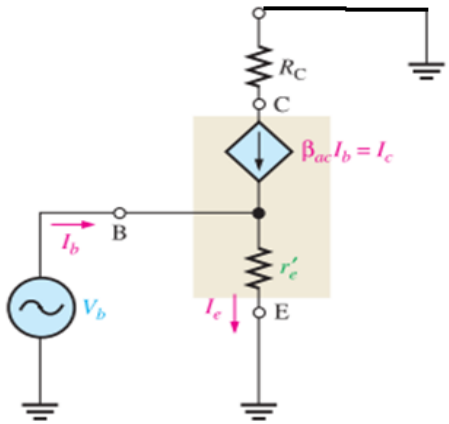
$$R_{in(base)} = \frac{V_{in}}{I_{in}} = \frac{V_b}{I_b}$$

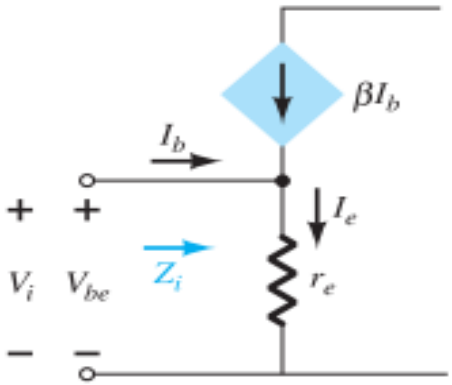
$$Z_i = \frac{V_i}{I_b} = \frac{V_{be}}{I_b}$$

$$V_{be} = I_e r_e = (I_c + I_b) r_e = (\beta I_b + I_b) r_e$$
$$= (\beta + 1) I_b r_e$$

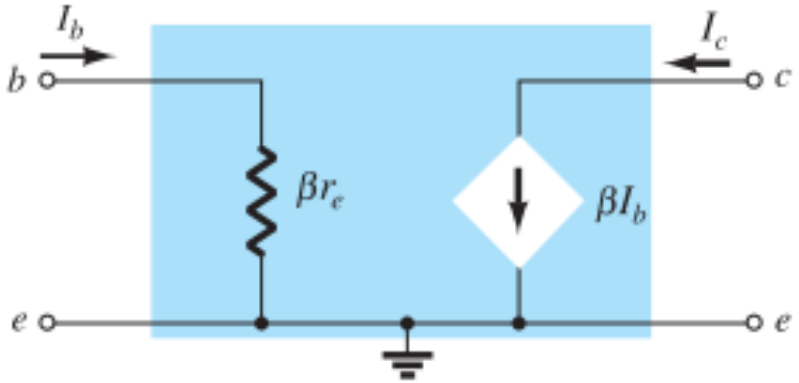
$$Z_i = \frac{V_{be}}{I_b} = \frac{(\beta + 1) I_b r_e}{I_b}$$

$$Z_i = (\beta + 1) r_e \cong \beta r_e$$





Improved BJT equivalent circuit.



- ✓ now the input and output circuits are isolated and only linked by the controlled source
- ✓ This form is much easier to work with when analyzing networks.

Output Characteristic

The output characteristic is not practically the same as assumed in the model with constant B curves

- ✓ Rather, they have a slope as shown In Fig. 5.15 that defines the output impedance of the device.
- ✓ The steeper the slope, the less the output impedance and the less ideal the transistor.
- ✓ In general, it is desirable to have large output impedances to avoid loading down the next stage of a design.

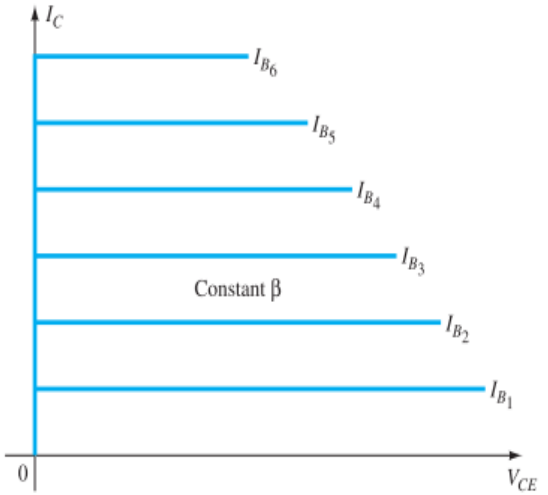


FIG. 5.11
Constant β characteristics.

$$r_o = \frac{\Delta V}{\Delta I} = \frac{V_A + V_{CE_Q}}{I_{C_Q}}$$

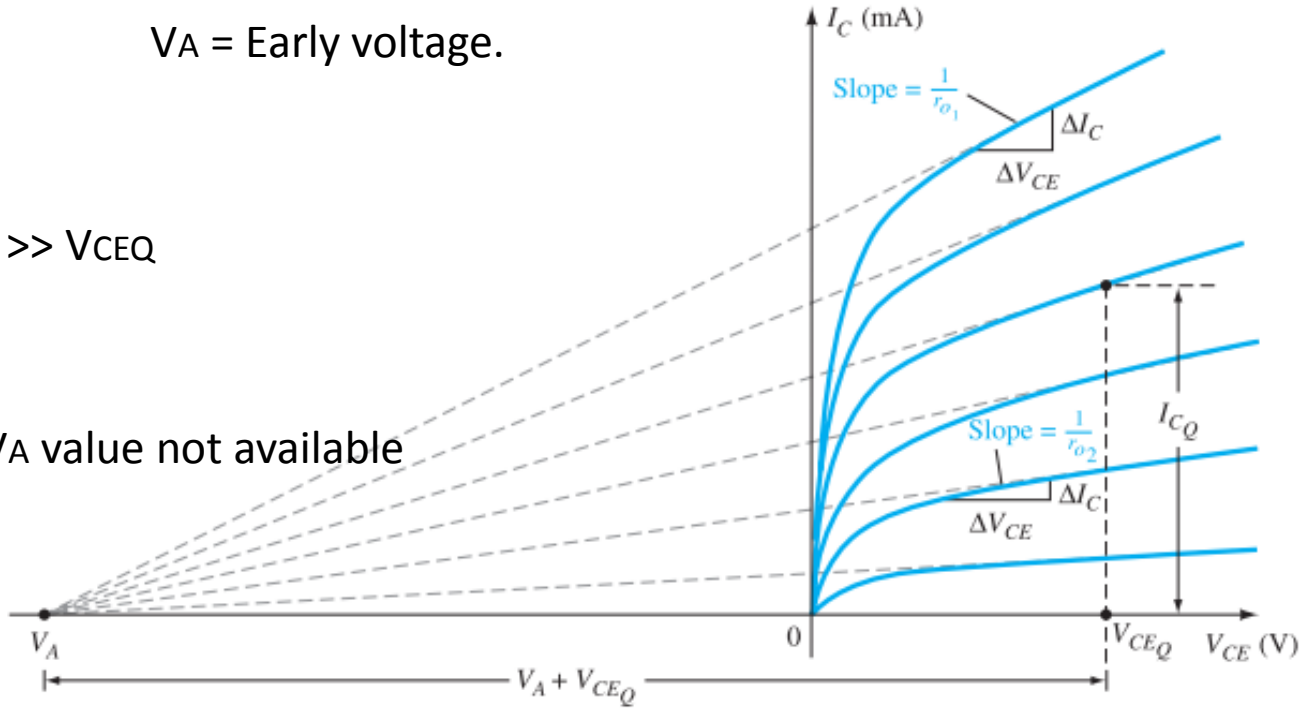
VA = Early voltage.

$$r_o \cong \frac{V_A}{I_{C_Q}}$$

VA >> VCEQ

$$r_o = \frac{\Delta V_{CE}}{\Delta I_C}$$

If VA value not available



Output Resistance

The output impedance will appear as a resistor in parallel with the output as shown in Fig. 5.16 .

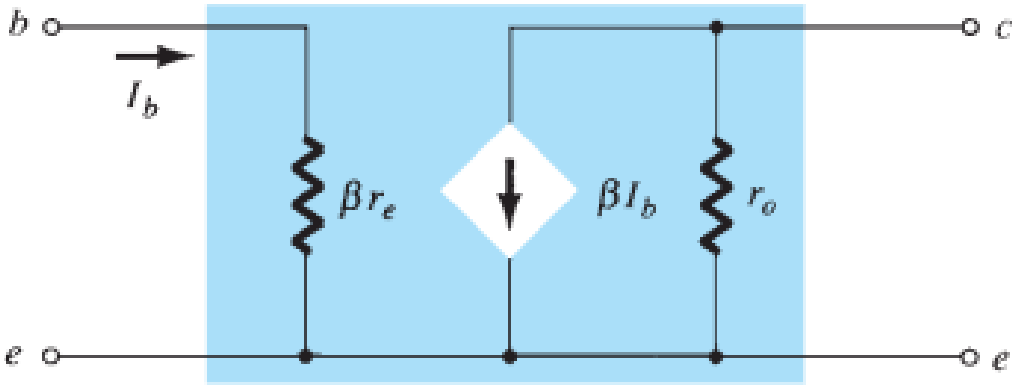


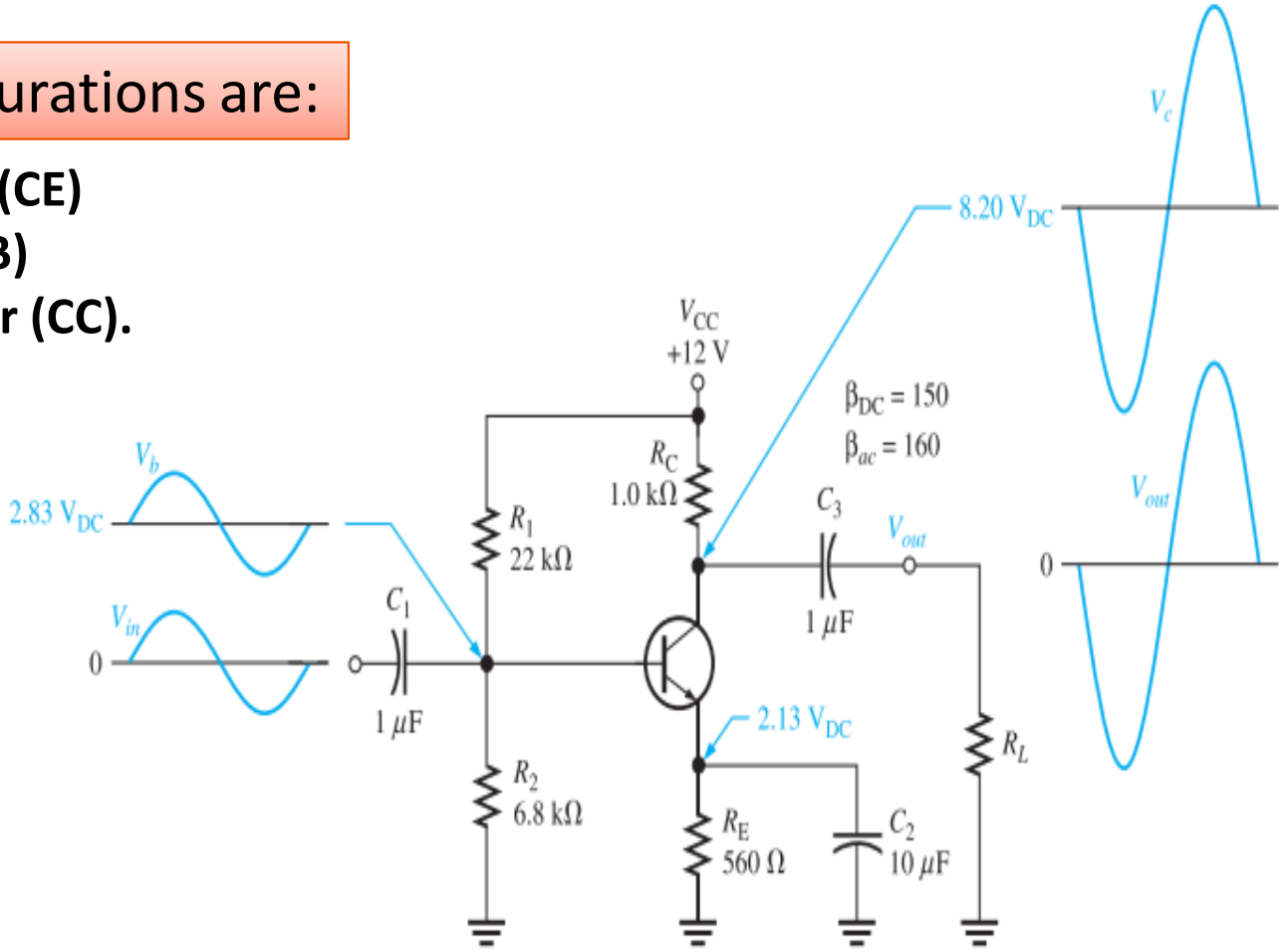
FIG. 5.16

r_e model for the common-emitter transistor configuration including effects of r_o.

6–3 The Common-Emitter Amplifier

Three amplifier configurations are:

1. **The Common-Emitter (CE)**
2. **The Common-Base (CB)**
3. **The Common-Collector (CC).**

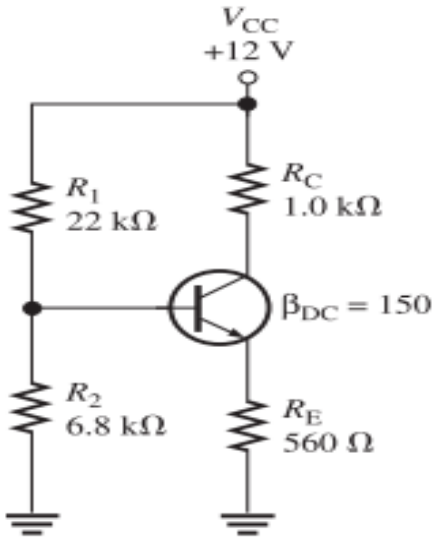


- ✓ The common-emitter (CE) configuration has the emitter as the common terminal, or ground, to an ac signal.
- ✓ CE amplifiers exhibit high voltage gain and high current gain.

6–3 The Common-Emitter Amplifier

- The figure shows a CE amplifier with voltage-divider bias and coupling capacitors C1 and C3 on the input and output and a **bypass capacitor**, C2, from emitter to ground.
- The input signal, Vin, is capacitively coupled to the base terminal,
- The output signal, V_{out}, is capacitively coupled from the collector to the load.

- ✓ The amplified output is 180^{o} out of phase with the input
- ✓ There is no signal at the emitter because the bypass capacitor effectively shorts the emitter to ground at the signal frequency.



- a dc equivalent circuit is developed by removing the coupling and bypass capacitors because they appear open as far as the dc bias is concerned.

$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2} = \frac{(6.8\,\text{k}\Omega)(22\,\text{k}\Omega)}{6.8\,\text{k}\Omega + 22\,\text{k}\Omega} = 5.19\,\text{k}\Omega$$

$$V_{TH} = \left(\frac{R_2}{R_1 + R_2}\right)V_{CC} = \left(\frac{6.8\,\text{k}\Omega}{6.8\,\text{k}\Omega + 22\,\text{k}\Omega}\right)12\,\text{V} = 2.83\,\text{V}$$

$$I_E = \frac{V_{TH} - V_{BE}}{R_E + R_{TH}/\beta_{DC}} = \frac{2.83\,\text{V} - 0.7\,\text{V}}{560\,\Omega + 34.6\,\Omega} = 3.58\,\text{mA}$$

$$I_C \cong I_E = 3.58\,\text{mA}$$

$$V_E = I_E R_E = (3.58\,\text{mA})(560\,\Omega) = 2\,\text{V}$$

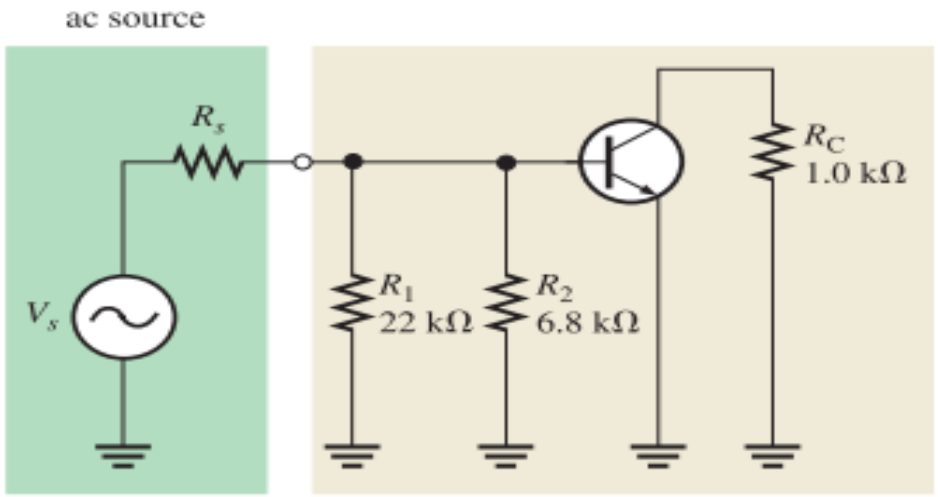
$$V_B = V_E + 0.7\,\text{V} = 2.7\,\text{V}$$

$$V_C = V_{CC} - I_C R_C = 12\,\text{V} - (3.58\,\text{mA})(1.0\,\text{k}\Omega) = 8.42\,\text{V}$$

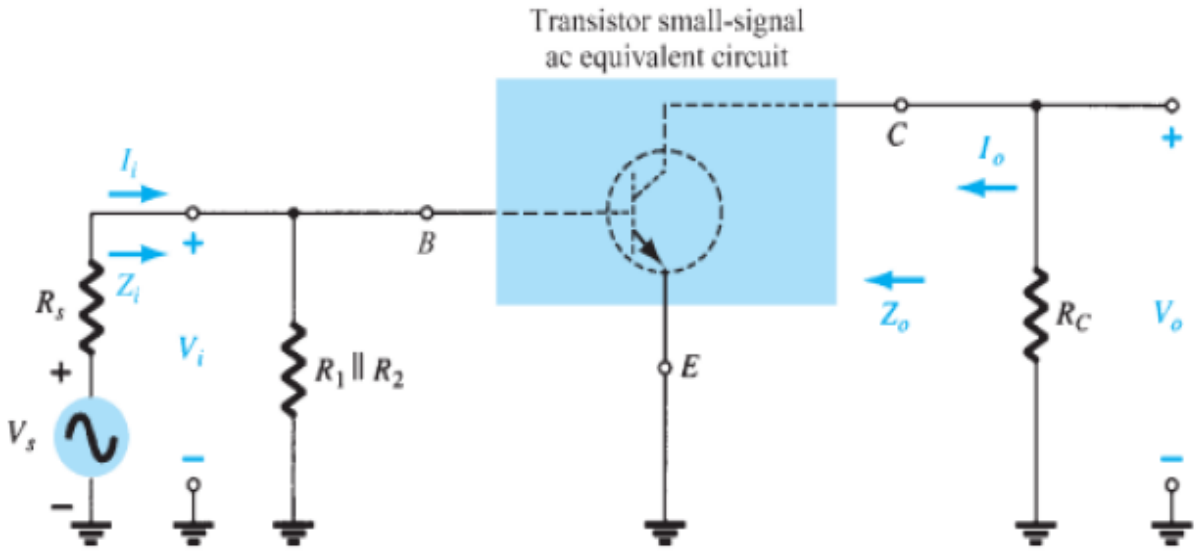
$$V_{CE} = V_C - V_E = 8.42\,\text{V} - 2\,\text{V} = 6.42\,\text{V}$$

an ac equivalent circuit is developed as

1. The capacitors C_1, C_2, and C_3 are replaced by effective shorts because their values are selected so that X_C is negligible at the signal frequency and can be considered to be 0 Ω.
2. The dc source is replaced by ground.



(b) With an input signal voltage



an ac equivalent circuit using the model

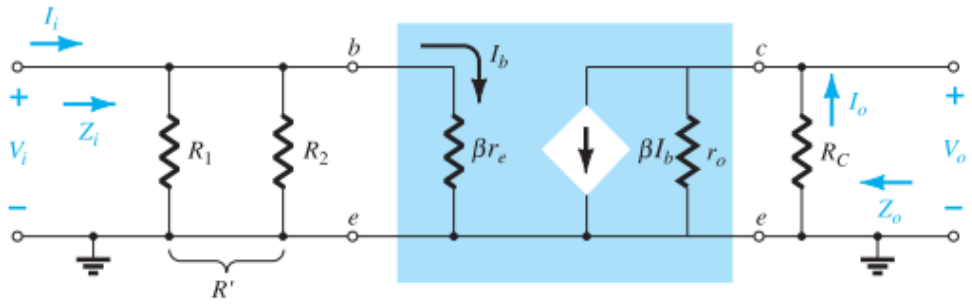
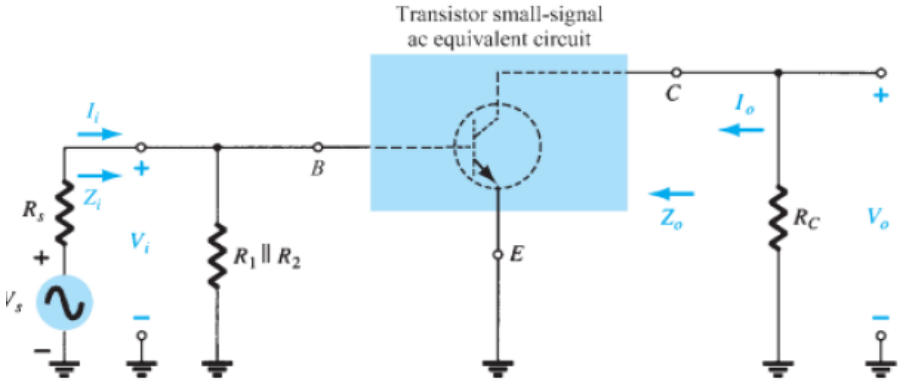


FIG. 5.27

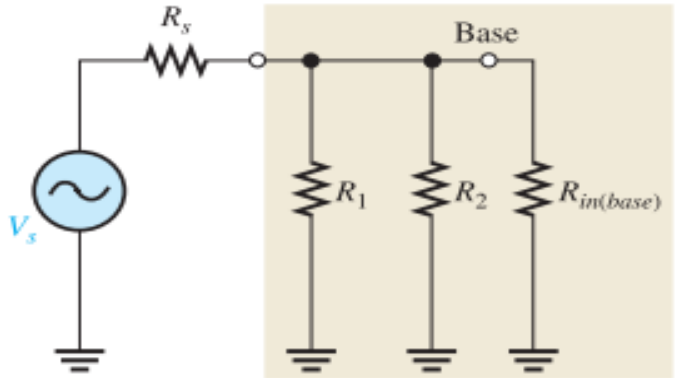
Substituting the r_e equivalent circuit into the ac equivalent network of Fig. 5.26.

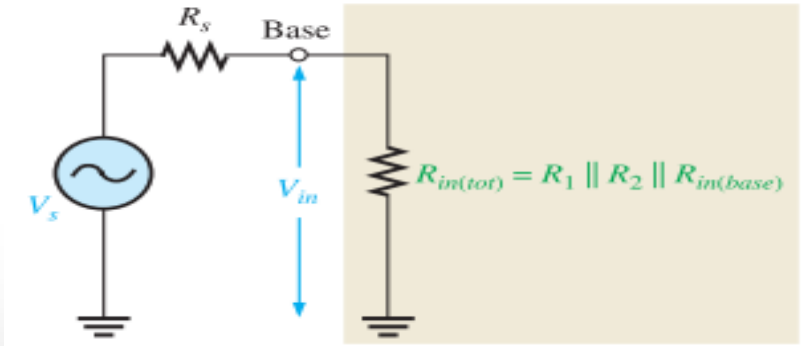


Total Input Resistance

is the resistance "seen" by an ac source connected to the input

$$R_{in(tot)} = R_1 \parallel R_2 \parallel R_{in(base)}$$

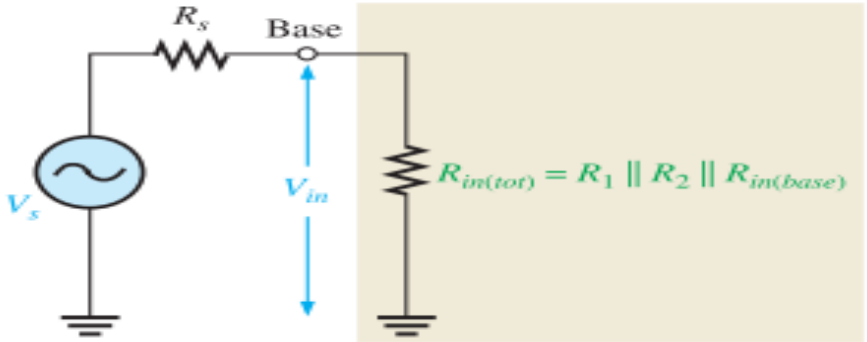




Signal (AC) Voltage at the Base

Two factors for determining the actual signal voltage at the base:

1. The source resistance (Rs),
2. The ac input resistance at the base of the transistor $R_{in(base)}$



✓ The signal voltage at the base of the transistor is found by the voltage-divider:

$$V_b = \left(\frac{R_{in(tot)}}{R_s + R_{in(tot)}}\right)V_s$$

A high value of input resistance is desirable so that the amplifier will not excessively load the signal source.

If $R_s \ll R_{in(tot)}$, then $V_b \cong V_s$ where V_b is the input voltage, V_{in}, to the amplifier.